AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of claims

Claim 1. (**Cancelled**)

Claim 2. (**Currently Amended**) ~~A system according to claim 1 and further comprising~~ A chip comprising:

at least two processing units with separate memories and separate busses, wherein said at least two processing units exchange data therebetween by transferring said data between said memories;

at least one first in first out (FIFO) unit ~~used by said processing units~~ to transfer said data ~~therebetween~~ between said busses;

at least one first direct memory access (DMA) channel to transfer said data from one of said memories to said at least one FIFO unit; and

at least one second DMA channel to transfer said data from said at least one FIFO unit to another of said memories.

Claim 3. (**Currently Amended**) A ~~system~~ chip according to claim 2 and further comprising [[a]] at least one data flow control unit ~~able to control~~ to regulate flow of said data ~~transfer~~ to and from said at least one FIFO unit.

Claim 4. (**Currently Amended**) A ~~system~~ chip according to claim [[1]] 2 wherein said processing units are central processing units (CPUs).

Claim 5. (**Currently Amended**) A ~~system~~ chip according to claim [[1]] 2 and further comprising at least two asynchronous clocks ~~controlling~~ to control said at least two processing units.

Claim 6. (**Currently Amended**) A ~~system~~ chip according to claim [[1]] 2 wherein one of said processing units is [[able]] to process media access control (MAC) commands and another of said processing units is [[able]] to process physical layer device (PHY) commands of a networking protocol.

Claims 7-25. (**Cancelled**)

Claim 26. (**Currently Amended**) A chip according to claim [[24]] 2 wherein said ~~first memory and said second memory~~ memories are [[RAM]] random access memories (RAMs).

Claim 27. (**Currently Amended**) A chip according to claim [[24]] 2 and further comprising a common register accessible by said ~~first processing unit and said second processing unit~~ processing units to act as a channel of communication by which said processing units are to coordinate exchange of said data between them.

Claims 28-35. (**Cancelled**)

Claim 36. (**Currently Amended**) A method for transferring data between processing units comprising:

~~first enabling at least one first CPU embedded on a chip to control writing of data to at least one FIFO generally concurrently with second enabling at least one second CPU embedded on said chip to control reading of said data from said at least one FIFO~~

sending data from a first processing unit embedded on a chip to a second processing unit embedded on said chip by establishing a first direct memory access (DMA) channel to a first in first out (FIFO) unit from a first memory directly accessible only by said first processing unit, and a second DMA channel from said FIFO unit to a second memory directly accessible only by said second processing unit.

Claim 37. (**Currently Amended**) A method according to claim 36, wherein operation of said first ~~enabling~~ DMA channel comprises any of the actions selected from the group consisting of:

~~instructing an apparatus to transmit data~~ transferring data from said first memory to said FIFO unit on request by said first processing unit;

~~checking if~~ waiting until said ~~at least one~~ FIFO unit is not full before ~~said writing~~ transferring each row of said data; and

~~checking if~~ notifying said first processing unit when all of said data has been ~~written~~ transferred to said FIFO unit.[[; and]]

~~transmitting a signal.~~

Claim 38. (**Currently Amended**) A method according to claim 36, wherein operation of said second ~~enabling~~ DMA channel comprises any of the actions selected from the group consisting of:

~~instructing an apparatus to receive data~~ transferring data from said FIFO to said second memory on request by said second processing unit;

~~checking if~~ waiting until said ~~at least one~~ FIFO unit is not empty before ~~said writing~~ transferring each row of said data; and

~~checking if~~ notifying said second processing unit when all of said data has been ~~written~~ transferred to said second memory.[[; and]]

~~receiving a signal; and~~

~~transmitting a signal.~~

Claim 39. (**Cancelled**)

Claim 40. (**Currently Amended**) A method according to claim [[39]] 36 wherein said first processing unit and said second processing unit are CPUs.

Claim 41. (**Currently Amended**) A method according to claim [[39]] 36 wherein said first memory and said second memory are [[RAM]] RAMs.

Claims 42-53. (**Cancelled**)

Claim 54. (**New**) A chip according to claim 2 wherein said first DMA channel and said second DMA channel are to operate substantially simultaneously.

Claim 55. (**New**) A method according to claim 36 wherein said first DMA channel and said second DMA channel are to operate substantially simultaneously.

Claim 56. (**New**) A device including a chip wherein said chip comprises:

at least two processing units with separate memories and separate busses, wherein said at least two processing units exchange data therebetween by transferring said data between said memories;

at least one first in first out (FIFO) unit to transfer said data between said busses;

at least one first direct memory access (DMA) channel to transfer said data from one of said memories to said at least one FIFO unit; and

at least one second DMA channel to transfer said data from said at least one FIFO unit to another of said memories.

Claim 57. (**New**) A device according to claim 56 wherein said chip further comprises at least one data flow control unit to regulate flow of said data to and from said at least one FIFO unit.

Claim 58. (**New**) A device according to claim 56 wherein said processing units are central processing units (CPUs).

Claim 59. (**New**) A device according to claim 56 wherein said chip further comprises at least two asynchronous clocks to control said at least two processing units.

Claim 60. (**New**) A device according to claim 56 wherein one of said processing units is to process media access control (MAC) commands and another of said processing units is to process physical layer device (PHY) commands of a networking protocol.

Claim 61. (New) A device according to claim 56 wherein said memories are random access memories (RAMs).

Claim 62. (New) A device according to claim 56 wherein said chip further comprises a common register accessible by said processing units to act as a channel of communication by which said processing units are to coordinate exchange of said data therebetween.

Claim 63. (New) A device according to claim 56 wherein said first DMA channel and said second DMA channel are to operate substantially simultaneously.